#0703

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30022/US/2	APPLICATION NO. Not ~~Yet Assigned~~
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales	10/631,742
		FILING DATE Concurrently Herewith	GROUP ART UNIT 2829 Not Yet ~~Assigned~~

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
EP	AA	5,975,958	11-02-99	Weidler	439	620	
EP	AB	6,021,499	02/01/00	Aleshi	713	300	
EP	AC	6,023,202	02-08-00	Hill	333	24	
EP	AD	6,109,971	08-29-00	Vadlakonda	439	620	
EP	AE	6,124,756	09-26-00	Yaklin et al.	327	564	
EP	AF	6,147,542	11-14-00	Yaklin	327	344	
EP	AG	6,249,171 B1	06-19-01	Yaklin et al.	327	382	

FOREIGN PATENT DOCUMENTS

N/A

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
EP	AH	00/45420	08/03/00	WO				
EP	AI	0 801 468 A2	10/15/97	EP				

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EP	AJ	Al-sarawi, Said F., "Wire Bonded Stacked Chips," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node35," January 25, 2002, pp. 1-2
EP	AK	Al-sarawi, Said F., "Blind Castellation Interconnection," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node44," January 25, 2002, p. 1
EP	AL	Al-sarawi, Said F., "Silicon Efficiency," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node20," January 25, 2002, pp. 1-2
EP	AM	Al-sarawi, Said F., "Delay," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node22," January 25, 2002, p. 1

EXAMINER	DATE CONSIDERED
Eva Perez	3-15-05

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30022/US/2	APPLICATION NO. Not Yet ~~Assigned~~ 10/631,342
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales	
		FILING DATE Concurrently Herewith	GROUP ART UNIT Not Yet ~~Assigned~~ 2826

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*		
EP	AN	Al-sarawi, Said F., "Noise," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node23," January 25, 2002, p. 1
EP	AO	Al-sarawi, Said F., "Power Consumption," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node24," January 25, 2002, p. 1
EP	AP	Al-sarawi, Said F., "Speed," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node25," January 25, 2002, p. 1
EP	AQ	Al-sarawi, Said F., "Interconnect Capacity," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node26," January 25, 2002, pp. 1-2
EP	AR	Al-sarawi, Said F., "Interconnection Capacity Between Packaging Levels," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node27," January 25, 2002, p. 1
EP	AS	Al-sarawi, Said F., "Stacked Tape Carrier," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node30," January 25, 2002, p. 1
EP	AT	Al-sarawi, Said F., "Solder Edge Conductors," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node31," January 25, 2002, pp. 1-2
EP	AU	Al-sarawi, Said F., "Thin Film Conductors on Face-of-a-Cube," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node32," January 25, 2002, pp. 1-2
EP	AV	Al-sarawi, Said F., "An Interconnection Substrate Soldered to the Cube Face," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node33," January 25, 2002, pp. 1-2

EXAMINER	DATE CONSIDERED
Eva Rust	3-15-05

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FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30022/US/2	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales 16/631,342	
		FILING DATE Concurrently Herewith	GROUP ART UNIT Not Yet Assigned 2826

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*		
EP	AW	Al-sarawi, Said F., "Folded Flex Circuits," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node34," January 25, 2002, p. 1
EP	AX	Al-sarawi, Said F., "Area Interconnection Between Stacked ICs," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node36," January 25, 2002, p. 1
EP	AY	Al-sarawi, Said F., "Flip-chip Bonded Stacked Chips Without Spacers," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node37," January 25, 2002, p. 1
EP	AZ	Al-sarawi, Said F., "Flip-chip Bonded Stacked Chips With Spacers," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node38," January 25, 2002, p. 1
EP	BA	Al-sarawi, Said F., "Microbridge Springs and Thermomigration Vias," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node39," January 25, 2002, p. 1
EP	BB	Agere Systems – About 1394, "1394 – The High-Speed Serial Interface for All the Right Reasons/1394 Driver Support," obtained from website http://www.agree.com/1394/about.html," January 25, 2002, p. 1
EP	BC	Press Release Tuesday October 17, 2000, "Lucent Technologies introduces low-power IEEE-1394A chip for high-speed connection between PCs and consumer electronic devices," obtained from website http://www.lucent.com/press/1000/001017.mea.html," January 25, 2002, pp. 1-3
EP	BD	1394 Trade Association: Technology, "1394 Technology," obtained from website http://www.1394ta.org/Technology/," January 25, 2002, p. 1
EP	BE	1394 Trade Association: Technology, "An Introduction to the Instrument and Industrial Control Protocol," obtained at website http://www.1394ta.org/Download/Technology/iicpPaper2.pdf," January 25, 2002, 6 pages
EP	BF	Apple Computer, Inc., "Firewire Technology Fact Sheet," obtained at website "http://a772.g.akamai.net/7/772/51/f7f756ae8e5bf0/www.apple.com/firewire/pdf/FireWireFS-b.pdf", March 13, 2002, pp. 1-4
EP	BG	McMunn, Lee James, "The Physical Layer," obtained at website "http://www.awstevenson.demon.co.uk/SYSNOTES/physic.htm," March 12, 2002, pp. 1-2
EP	BH	Willis, P. J., "Communication Protocols," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/chapter2_6.html," August 17, 2001, p. 1

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30022/US/2	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales	10/631,342
		FILING DATE Concurrently Herewith	GROUP ART UNIT Not Yet Assigned 2826

SP	BI	Willis, P. J., "The OSI Model," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/sections2_6_1.html," August 17, 2001, p.1
SP	BJ	Willis, P. J., "Physical Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/subsection2_6_1_1.html," August 17, 2001, p. 1
SP	BK	Willis, P. J., "Data Link Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/subsection2_6_1_2.html," August 17, 2001, p.1
SP	BL	Willis, P. J., "Network Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/subsection2_6_1_3.html," August 17, 2001, p.1
SP	BM	Willis, P. J., "The Physical Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/section2_7_1.html," August 17, 2001, pp. 1-2
SP	BN	Willis, P. J., "The Datalink Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/section2_7_2.html," August 17, 2001, pp. 1-2
SP	BO	Embedded Systems Programming, "Fundamentals of Firewire," obtained at website "http://www.embedded.com/1999/9906/9906feat2.htm," August 28, 2001, pp. 1-14
SP	BP	Microprocessor and Microcomputer Standards Committee of the IEEE Computer Society, "P1394a Draft Standard for a High Performance Serial Bus (Supplement)," The Institute of Electrical and Electronics Engineers, Inc., June 30, 1999, pp.1-27
SP	BQ	Lucent Technologies, Inc., "IEEE 1394 Isolation," Application Note, November 1998, obtained at website "http://www.agere.com/1394/docs/AP98074-01.pdf," pp. 1-16

EXAMINER	DATE CONSIDERED
Sion Quinlan	3-15-05

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#0107

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30022/US/2 (500986.03)	APPLICATION NO. 10/631,342
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales	
		FILING DATE July 30, 2003	GROUP ART UNIT 2826 Not yet assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
EP	AA	5,027,253	06/25/91	Lauffer et al.	361	321	
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AK							
	AL							
	AM							
	AN							
	AO							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

EP	AP	IBM Technical Disclosure Bulletin NN8712167, "Decoupling Capacitor Structure to Reduce FET Output Driver Switching Noise", December 1, 1987, pages 167-168.
EP	AQ	IBM Technical Bulletin NN85014857, "Clipped Decoupled Twin-Carrier Module for IC Memory Chips", January 1, 1985, page numbers 4857-4858.

EXAMINER	DATE CONSIDERED
[signature]	3-15-05

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

#0704

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500986.03	APPLICATION NO. 10/631,342
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales	
		FILING DATE July 30, 2003	GROUP ART UNIT ~~2829~~ 2826

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
SS	AA	5,068,708	11/26/91	Newman	257	668	
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AK							
	AL							
	AM							
	AN							
	AO							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AP	
	AQ	
	AR	

EXAMINER	DATE CONSIDERED
ER	3/15/05

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